





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Substitute for form 1449A/B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	August 6, 2003
				First Named Inventor	Kie Y. Ahn
				Art Unit	2836
				Examiner Name	S. Jackson
Sheet	1	of	1	Attorney Docket Number	M4065.0254/P254-B

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
<i>[Signature]</i>	*AA	5,070,317	12/3/1991	Bhagat	361 / 336 / 200
<i>[Signature]</i>	*AB	5,279,988	1/18/1994	Saadat et al.	438 / 3
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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
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NON PATENT LITERATURE DOCUMENTS				
Examiner Initials [*]	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
	CA	Mimura et al.; "System module: a new Chip-On-Chip module technology"; IEEE , 1997, Custom Integrated Circuits Conference, pages 439-442.		
	CB	Yan et al.; "Reducing Operating Voltage from 3, 2, to 1 Volt and Below – challenges and guidelines for possible solutions"; IEEE, 1995, IEDM, pages 55-58.		
	*CC	Christensen et al.; "Wafer Through-Hole Interconnections with High Vertical Wiring Densities", IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part A, Vol. 19, No. 4, Dec. 1996, pages 516-522.		
	*CD	Mimura et al.; "System module: a new Chip-On-Chip module technology"; IEEE , 1997, Custom Integrated Circuits Conference, pages 439-442.		

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Stephen Jackson

8-19-04